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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,668	01/17/2002	Patrick L. Connor	PW 0249740 P12832	1163
7590 04/02/2007				
Pillsbury Winthrop LLP Intellectual Property Group Suite 2800 725 South Figueroa Street Los Angeles, CA 90017-5406		EXAMINER PATEL, NIRAV B		
		ART UNIT 2135		PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MONTHS	04/02/2007	PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/051,668	CONNOR ET AL.	
	Examiner	Art Unit	
	Nirav Patel	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 January 2007 (RCE).
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 8-13, 16, 18, 19, 21, 22, 24, 25, 27, 34 and 35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 8-10, 12, 16, 18, 21, 22, 24, 27, 34 and 35 is/are rejected.
- 7) ☒ Claim(s) 11, 19, 25 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Applicant's submission for RCE filed on January 16, 2007 has been entered.
2. Claims 8-13, 16, 18, 19, 21, 22, 24, 25, 27, 34 and 35 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 8, 9, 13, 16, 22, 27 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishna, Suresh (WO 01/05086) in view of Johnson et al (US Patent No. 6,754,755) and in view Brcich et al (US Patent No. 6,304,911).

As per claim 8, Krishna discloses host memory to store the encrypted packet [Fig. 1A, 1B, page 7 lines 34-35], a controller to receive the encrypted packet and to perform said decryption operation [Fig. 1A, 1B, component 102 or 152, Fig. 3, 6A, page 9 lines 1-2, page 18 lines 30-31], a bus providing electronic communication among said host memory and said controller [Fig. 1A, 1B, page 7 lines 16-20]. Krishna teaches that receiving the packets from the LAN or WAN, and **storing the packets to the memory 166 and transferring to the chip 152** on the service module 153 for **security processing (e.g. decryption/authentication)**. The processed packets are

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then sent back over the matrix 154 through the memory 166 [Fig. 1B, 6A, page 7 lines 34-36, page 8 lines 1-2, page 18 lines 30-31]. Krishna teaches the transferring process of the packet between the host memory and the controller [Fig. 1B, page 7 lines 34-36, col. 8 lines 1-2 i.e. transferring from the host memory to the controller and transferring back from the controller to the host memory].

Johnson teaches:

a network driver to regulate the various operation and to transmit a command [Fig. 5, 6 col. 11 lines 63-66], the controller asserting an interrupt after the delay time/value has been occurred (i.e. latency value) [Fig. 2, 5, col. 9 lines 22-40].

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Johnson with Krishna, since one would have been motivated to improve network processing between the network adapter or NIC and its host computer [Johnson, col. 4 lines 26-28].

Krishna and Johnson don't expressively mention the interrupt latency value being based on a number of bytes of the packet upon which an action has been performed.

Breich teaches:

a network peripheral which includes a controller, a memory management unit, data storage unit a host system interface and network interface [Fig. 4]. Further, the host system interface couples to a host system bus and provides for the transfer of data between the host system bus and the network peripheral [Fig. 4, col. 9 lines 56-65].

The network peripheral determines the interrupt handler latency value and the interrupt handler latency value being based on a number of bytes of the packet upon which an

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action has been performed and said controller asserting an interrupt after the interrupt handler latency value has been occurred and before the decrypted packet has been transferred back from the controller to the host memory (i.e. before the packet transfer from the controller to the host memory) [**col. 4 lines 27-32, col. 14 lines 23-29, col. 12 lines 3-10, 40-44, Fig. 7**].

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Brcich with Krishna and Johnson, since one would have been motivated to provide an interrupt, so that a processor unit does not have to remain idle during the execution of an interrupt service routing for processing an incoming packet [**Brcich, col. 4 lines 9-12**].

As per claim 9, the rejection of claim 8 is incorporated and further Krishna teaches:

network interface to provide electronic communication between said computer and a network [**page 6 lines 16-18 “as shown in Fig. 1, the cryptography acceleration chip 102 may be part of an otherwise standard network line card 103 which includes a WAN interface 112 that connects the processing system 100 to a WAN, such as the internet”**]. Further, Brcich teaches the physical interface to provide electronic communication between said computing system and a network [**Fig. 4**].

As per claim 13, the rejection of claim 8 is incorporated and further Krishna teaches the transferring process of the packet between the host memory and the controller [**Fig. 1B**,

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page 7 lines 34-36, col. 8 lines 1-2 i.e. transferring from the host memory to the controller and transferring back from the controller to the host memory].

Brich teaches interrupt handler latency value is based on a specific number of bytes being transferred and the interrupt is asserted after the specific number of bytes have been transferred **[Fig. 7, 16, col. 14 lines 23-29, col. 18 lines 37-48]**.

As per claim 16, it encompasses limitations that are similar to limitations of claim 8. Thus, it is rejected with the same rationale applied against claim 8 above.

As per claim 22, it encompasses limitations that are similar to limitations of claim 8. Thus, it is rejected with the same rationale applied against claim 8 above.

As per claim 27, the rejection of claim 22 is incorporated and it encompasses limitations that are similar to limitations of claim 13. Thus, it is rejected with the same rationale applied against claim 13 above.

As per claim 34, the rejection of claim 16 is incorporated and it encompasses limitations that are similar to limitations of claim 13. Thus, it is rejected with the same rationale applied against claim 13 above.

4. Claims 10, 12, 18 21, 24 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishna, Suresh (WO 01/05086) in view of Johnson et al (US Patent No. 6,754,755) and in view Brcich et al (US Patent No. 6,304,911) and in view of Hausman et al (US Patent No. 5,412,782).

As per claim 10, the rejection of claim 8 is incorporated and further Brcich teaches said interrupt handler latency value is based on a specific number of bytes **[Fig. 7, 16]**.

Hausman teaches said interrupt handler latency value is based on a specific number of bytes that have been transferred to the controller from the host memory and the interrupt is asserted after the specific number of bytes have been transferred to the controller **[Fig. 1, 5, col. 7 lines 31-67, col. 1 lines 48-56]**.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Hausman with Krishna, Johnson and Brcich, since one would have been motivated to provide high throughput for hosts of a network **[Hausman, col. 1 lines 8-10]**.

As per claim 12, the rejection of claim 10 is incorporated and it encompasses limitations that are similar to limitations of claim 10. Thus, it is rejected with the same rationale applied against claim 10 above.

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As per claim 18, the rejection of claim 16 is incorporated and it encompasses limitations that are similar to limitations of claim 10. Thus, it is rejected with the same rationale applied against claim 10 above.

As per claim 21, the rejection of claim 18 is incorporated and it encompasses limitations that are similar to limitations of claim 12. Thus, it is rejected with the same rationale applied against claim 12 above.

As per claim 24, the rejection of claim 22 is incorporated and it encompasses limitations that are similar to limitations of claim 10. Thus, it is rejected with the same rationale applied against claim 10 above.

As per claim 35, the rejection of claim 24 is incorporated and it encompasses limitations that are similar to limitations of claim 12. Thus, it is rejected with the same rationale applied against claim 12 above.

Allowable Subject Matter

5. Claims 11, 19 and 25 are objected to as being dependent upon a rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Amendment

6. Applicant's submission for RCE filed on January 16, 2007 has been entered. Applicant has amended claims 8-13, 16, 18, 19, 21, 22, 24, 25, 27 and added new claims 34 and 35, which necessitated new ground of rejection. See rejection above.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure (See form 892).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nirav Patel whose telephone number is 571-272-5936. The examiner can normally be reached on 8 am - 4:30 pm (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached on 571-272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

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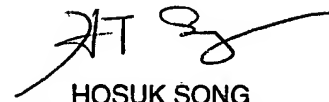
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USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NBP

3/21/07


HOSUK SONG
PRIMARY EXAMINER